1. The $\ell$-exclusion problem is a variant of mutual exclusion, where at most $\ell$ processors can enter the critical section simultaneously. Design an algorithm for this problem using a single RMW register. State and prove the liveness condition that your algorithm satisfies.

2. Consider the following executions of three processors $A$, $B$ and $C$ on a single read/write object $X$, and argue whether they are quiescently consistent, sequentially consistent or linearizable.

   (a) Execution 1

   A ------------[read(X)-----return(X,1)]----------------------------------------------------

   B -----[write(X,1)-------------------ack(X)]----[read(X)-----return(X,2)]--

   C ------------[write(X,2)---------ack(X)]---------------------------------------------------

   (b) Execution 2

   A ------------[read(X)-----return(X,1)]----------------------------------------------------

   B -----[write(X,1)-------------------ack(X)]----[read(X)-----return(X,1)]--

   C ------------[write(X,2)---------ack(X)]---------------------------------------------------

3. We say that a property is *compositional* if, whenever each object in the system satisfies the property, the entire system satisfies the property.

   (a) Prove, using a counter-example, that sequential consistency is not compositional.

   (b) Prove that quiescent consistency is compositional. In other words, given any execution $\sigma$, if, for each object $X$, $\sigma \mid X$ satisfies QC, then $\sigma$ satisfies QC.

   (c) Linearizability is also compositional, i.e., if for each object $X$, $\sigma \mid X$ is linearizable, then $\sigma$ is linearizable. Prove that the converse is also true, i.e., if $\sigma$ is linearizable, then for all objects $X$, $\sigma \mid X$ is also linearizable.